Design & Simulation of Analog Phase Lock Loop with Ring oscillators Using 0.18μm CMOS Technology

Dr. Partha Pratim Sahu1, Manish Kumar2
1Dept. of Electronics & Communication, Tezpur University, Assam, India
2Dept. of Electronics & Communication, Tezpur Central University, Assam, India
Email: manish_earn@yahoo.co.in

Abstract: This brief discusses the challenges and present techniques in designing analog phase-locked loops in nanometer CMOS. Phase Locked Loops are used in every communication system. Some of its uses include recovering clock from digital data signals, performing frequency, phase modulation and demodulation, recovering the carrier from satellite transmission signals and as a frequency synthesizer. There are many designs in communication that require frequency synthesizer to generate a range of frequencies; such as cordless telephones, mobile radios and other wireless products. The accuracy of the required frequencies is very important in these designs as the performance is based on this parameter. One approach to this necessity could be to use crystal oscillators. It is not only impractical, but is impossible to use an array of crystal oscillators for multiple frequencies. Therefore some other techniques must be used to circumvent the problem. The main benefit of using Phase Locked Loop technique in frequency synthesizers that it can generate frequencies comparable to the accuracy of a crystal oscillator and offer other advantages mentioned previously. For this reason most of the communication design make use of a PLL frequency synthesizer. Considering the scope of this single circuit, Phase locked loop is an excellent research topic as it covers many disciplines of electrical engineering such as Communication Theory, Control Theory, Signal Analysis, Noise Characterization, design with transistors and op-Amps, Digital Circuit design and non-linear circuit analysis. I am using .35um CMOS Technology. I am using microwave office tools (AWR) to implement this work.

Keywords: Voltage Controlled Oscillator (VCO), Loop Filter, Phase-Locked Loop (PLL), Charge Pump, Ring Oscillator, NMOS, PMOS.

I. INTRODUCTION

Phase-locked loop (PLL) is perhaps the most widely used mixed-signal circuit block in a system-on-chip. Phase-locked loops (PLLs) find wide applications in many areas such as communication systems, wireless systems, digital circuits, power systems and disk drives. PLL is the choice circuit for applications like frequency synthesizers and clock recovery circuits (CRC) in communication. In the frequency synthesizer, the PLL enables the generation of a stable periodic waveform whose frequency can be varied over a wide range in small frequency steps. A PLL with a relatively narrow bandwidth is used to minimize the effect of the input jitter on the recovered clock. In the design of the transceiver, there is a clear trend towards full integration of the radio-frequency (RF) front end on a single die for the purpose of low cost and low power[3]. The design of RF building blocks in a CMOS process is now an important research topic in order to replace the more expensive bipolar process. The use of a sub micrometer CMOS process for the RF circuits enables the circuits to incorporate the digital baseband processing circuit on the same chip. The emergence of the sub micrometer CMOS technology has resulted in many high speed PLLs being implemented in CMOS technology. However, due to technology limitations on the passive component quality.

II. RF FUNDAMENTALS

Radio frequency (RF) waves are used in a wide range of communications, including radio, television, cordless phones, wireless LANs, and satellite communication. RF is around everyone and everything, and comes in many forms. RF energy is emitted from the numerous devices that use it for various types of communications. For the most part, it is invisible to humans. There is so much of it around, if you could actually see RF, it would probably scare you. Don't let it scare you[7], however, because the amount of regulated RF power transmitted from the devices used in daily lives is harmless. [10] Studies have shown that the amount of power emitted from many of these devices, such as cordless telephones or wireless network adapters, will not cause any physical harm if the devices are manufactured based on the maximum regulated power allowed for the device. Remember, RF consists of high frequency alternating current (AC) signals passing over a copper cable connected to an antenna. This antenna will then transform the received signal into radio waves that propagate through the air.

III. CMOS TECHNOLOGY & RF MODELS

In CMOS (Complementary Metal-Oxide-Semiconductor) technology, both N-type and P-type transistors are used to realize logic functions. Today, CMOS technology is the dominant semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs)[10]. The main advantage of CMOS over NMOS and bipolar technology is the much smaller power dissipation. Unlike NMOS or bipolar circuits, a CMOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows to integrate many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. The following applets demonstrate the N-type and P-type transistors used in CMOS technology, the basic CMOS inverter, NAND and NOR gates, and an AOI32 complex gate.

III.1 BSIM3

BSIM3 has been the most-used mainstream MOSFET model since the end of the 90s. There are three main versions of it, but basically only the third version has been used, in other words BSIM3[9]. This last version has a number of subversions as well. BSIM3 is attempting to have a model with a physical basis and still maintain the mathematical fitness of the previous model generations. BSIM3 is said to be a third-generation model. The number of model parameters is very large.

IV. PHASE LOCK LOOP

Phase Locked Loops (PLL) are a new class of circuit, used primarily in communication applications. It is suitable for a wide variety of applications, such as AM radio receivers, frequency demodulators, multipliers, dividers, and as frequency synthesizers. Now a whole PLL circuit can be
integrated as a part of a larger circuit on a single chip. This chapter gives a brief introduction to the basics of Phase Locked loops. The circuit configuration shown in Figure 1

V. PHASE DETECTOR

Phase detectors that are only sensitive to phase are the most straightforward form of detector. They simply produce an output that is proportional to the phase difference between the two signals. When the phase difference between the two incoming signals is steady, they produce a constant voltage. When there is a frequency difference between the two signals, they produce a varying voltage. In fact the simplest form of phase only sensitive detector is a mixer. From this it can be seen that the output signal will be have sum and difference signals.

CHARGE PUMP The term 'charge pump' is also used in phase-locked loop (PLL) circuits. This is a completely different application. In a PLL the phase difference between the reference signal (often from a crystal oscillator) and the output signal is translated into two signals - UP and DN.

VII. LOW PASS FILTER

A simple passive loop filter consists of a resistor that is connected in series with a capacitor. The resistor influences the bandwidth of the loop, whereas the capacitor controls the damping. A low pass filter is an electronic filter that passes low frequency signals but attenuates signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies from filter to filter. It is sometimes called a high-cut filter, or treble cut filter when used in audio applications. A low-pass filter is the opposite of a high-pass filter.

PORT
P=2
Z=50 Ohm
PORT P=1
ID=R1
Z=50 Ohm
R=1 Ohm

R = 2^\sqrt{f_\text{in}} \times C_1
R = (2*\sqrt{0.707})/714*62.2

Fig. 6 Circuit Design of LPF In PLL
to increased sensitivity to the power supply noise. Phase Noise varies typically by 3dB with temperature, in the -55°C to +85°C range.

VIII.I DESIGN AND SIMULATION RESULT OF VCO

Gen:Bc35:pmc&1
Gen:Bc35:pmc&1
Gen:Bc35:pmc&1
ID=M1    ID=M2VDD    ID=M3    ID=M4

Fig 7 DB(|S(1,1)|) Of LPF

Fig 8 DB(|S(2,1)|) Of LPF

VIII. VOLTAGE CONTROLLED OSCILLATOR (RING OSCILLATOR)

The ring oscillator can become affected in a number of ways: First, the low supply voltage puts an absolute limit on the voltage swing of the oscillator, thus degrading its phase noise [1]. It also limits the tuning signal range. This in turn increases the gain of the oscillator to support a given tuning range. The effects of high oscillator gain. High Pushing (change of the oscillation frequency with supply voltage) can cause Phase Noise degradation due
IX. SIMULATION RESULTS OF PLL DESIGN

Fig 15 Jitter Value of PLL

Fig 13. Voltage Time Response

Fig 14. Lock indication and control voltage

CONCLUSION & FUTURE WORK

This thesis describes a wide range of techniques employed in phase-locked loop. The investigation covers building blocks of the phase-locked loop, which are the VCO. The implementation of a proposed multi-band phase-locked loop was accomplished in this thesis work. This research was motivated by the necessity for integrated multi-band for use in multi-standard transceivers. The multi-band PLL uses a switched tuning VCO that allows a wide frequency range with a low conversion gain. Experimental results show that the PLL. The importance of optimizing the loop bandwidth in order to achieve the best phase noise performance for a phase-locked loop was shown. The impact of the noise generated from the resistor in the loop filter was highlighted. The subject of phase locked loop is wide and diverse. There are many other aspects that can be combined in the design to achieve better performance and more powerful. Consider for instant incorporating Fault Tolerant Design Techniques to a PLL design. Since recent advances in VLSI technology has made it possible to put complex digital circuits on a single chip, more and more circuits are now combined on a single chip to make a system as compact as possible, such as a PLL in a transceiver chip. As a result of this capability, it is very hard to locate an error in the event if the output of a system is not the expected one. Some of such system are related to critical application, where it is necessary that the system operates reliably, even under the circumstances that one of the major component fails. The design techniques that make it possible for a system to be operational even under the condition of failure are termed as Fault Tolerant Design Techniques and the system as the Fault Tolerant system.

If we add the divider circuit between phase detector and vco it will become frequency synthesizers.

REFERENCES


