Study on Optoelectronic-VLSI

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Abstract: VLSI-optoelectronics, also called smart-pixel technology, exploits the respective strengths of optics and electronic processing for the production of optical information processing systems of high performance. The recent integration of micron-size optoelectronic components such as emitters, photo detectors and spatial light modulators within VLSI electronic chips allows the fabrication of on/off chip data communication rate systems of the order of 1012 pin-Hz. Optoelectronic-VLSI (OE-VLSI) technology represents the familiar integration of photonic devices with silicon VLSI. It will be review the motivations and status of emerging OE-VLSI technologies and examine the performance of OEVL Technology versus conventional wire-bonded OE packaging. The results suggest that OE-VLSI integration offers substantial power and speed improvements even when relatively small numbers of photonic devices are driven with commodity complementary metal–oxide–semiconductor logic technologies.

Keywords—Small-pixel technology; Optical interconnect; Circuit modeling.

1. Introduction

Over the last 15 years, the optoelectronic community has witnessed a constant drive towards the full integration of optoelectronic components within their associated VLSI electronic processing circuitry. This trend originally fuelled by the long-haul telecommunications industry. Optoelectronics-VLSI (OE-VLSI) technology provides close integration of photonic devices with VLSI electronics. The goal is to supply multiple high-performance optical inputs and output signals, with aggregate data-rates up to and even exceeding a terabit-per-second, to state-of-the-art VLSI circuits. OE-VLSI technologies are used most effectively in systems where a high-bandwidth “data-fire hose” must be received, switched or quickly processed by the electronic circuit, and communicated out of the subsystem.

Such a technology allows a significant increase in integration density over all-electrical systems because the functionality present in many separate electronic chips can be condensed into fewer chips (and in some cases one single chip) with large numbers of optical inputs and/or outputs (I/Os). The use of OE-VLSI “packaging” simultaneously affords a reduction in the energy required to transmit digital signals within the system (and hence the power-delay product of the system) by reducing (and in certain cases eliminating) the parasitic associated with conventional packaging technology that use wire-bonds between chips. This permit an increase in interconnect speed for a given power dissipation today, demonstrators based on this technology exhibit the same aggregate bandwidth as that foreseen with electronic systems for the Year 2007. This remarkable achievement is rendered possible by a variety of factors the integration of micron-size optoelectronic transceivers with VLSI circuits the massive parallelism offered by free-space optics a better understanding of the added-value of optics in information processing systems; and the progress in low-cost optical assembly, testing and packaging.

In all these domains, however, technological issues mar the full potential of this technology, the interface of optoelectronics with silicon-based VLSI circuits is still technologically immature; the alignment and fabrication limitations faced by free-space optical components could be bettered by the adoption of existing solutions and established standards; the slow progress in adopting optics in computer architecture is symptomatic of the general lack of knowledge of optics by computer scientists as well as the ignorance of computer science by optical engineers. In short overall system required expert with different backgrounds.

2. Optoelectronics VLSI Component

All smart-pixel devices, irrespective of their related electronic logic family and optoelectronic interface, receive, modulate or emit information in the optical. Physical or functional diagram is shown in fig 1.

The VCSEL chip contains an 8x8 array of top-emitting VCSELs with a 250 µm pitch grown on a GaAs substrate. Each VCSEL consists of a single quantum well active region surrounded by distributed Bragg reflectors, and has been ion implanted for current confinement in the active region.

The threshold currents of the VCSELs are between 2.5 and 3.0 mA, the operating currents are less than 8 mA at 2 V, and the output powers are approximately 1 mW. 90 µm square bonding pads for attachment of the flip-chip bonds are evenly interspersed amongst the VCSELs, each pad located a distance of 125 µm (center-to-center) from its associated laser element. The silicon (CMOS) chip contains an 8x8 processing element (PE) array, an 8x8 photo receiver array, an 8x8 VCSEL driver array, and a 9x15 bonding pad array. Details of the three 8x8 arrays are given in the following paragraphs [2].
3. Smart Pixel And OE-VLSI Technology

The name smart pixel is combination of two idea “pixel” is an image processing term denoting a small part, or quantized fragment of an image, the word "smart" is coined from standard electronics and reflects the presence of logic circuits. Together they describe a myriad of devices.

As the smart pixel technology continues to evolve, there needs to be a basic understanding and acceptance of key performance metrics including connection density, complexity, and aggregate capacity [3].

Smart-pixel technologies can be applied materials with widely differing properties for light detection, logic, and also optical transmission. Various smart pixel technologies are currently being developed. Most smart pixels are based on either silicon or gallium arsenide substrates material. The main logic families being considered are silicon CMOS, silicon bipolar, and GaAs MESFET’s. As silicon–germanium technology matures, this will also become a prime candidate for integration with photonic devices. Various light detectors, transceiver circuits, and light transmitter device technologies have also been proposed.

OE-VLSI represents a generalization of smart-pixel technologies, in that the concept of each optical Input Output channel being associated with only a specific subset of transistors on the chip (i.e., a pixel) is replaced with a more comprehensive view of a technology that provides surface-normal optical interconnects to VLSI circuits through either monolithic or hybrid integration methods. Compared to high-performance all-electronic systems, OE-VLSI circuit technologies can offer a relatively simple means of communicating large amounts of information to-and-from a custom VLSI circuit, as well as a relative ease-of-design of the array. Indeed, one can show that a specific OE-VLSI technology can be expected provide an I/O bandwidth to a chip that grows in proportion to its computational bandwidth, even for ultra dense CMOS VLSI [4]. Such technologies have spawned a number of applications in high-performance computing and communications systems [5]. One factor in determining the suitability of a smart-pixel or OE-VLSI technology to a given application is the light transmitter technology that is adopted. Three approaches are presently under investigation: laser sources, LED sources, and light modulators. The first approach has the advantage in that active light sources such as vertical-cavity surface-emitting lasers (VCSEL’s) can provide large dynamic range and high contrast ratios [6]. The optical system can also be simplified because no external laser is required. Surface emitting lasers can be designed (with additional beam-shaping elements when necessary) to efficiently direct the laser beam out of the smart pixel. When arrays of lasers are integrated on a chip, substantial on-chip static power dissipation can ensue when the lasers are biased above threshold. Although some ultralow threshold devices are now being researched, VCSEL currently require threshold currents on the order of 100 A to

4. OE-VLSI Integration v/s Wirebonding

The most widely used means of providing electrical connections between electronic driver or receiver circuits and optical devices such as modulators and lasers, is wirebonding. A short-wire bond can provide a simple and cost effective means of connecting the photonic devices to the transceivers electronics. It is generally believed that the number of wire-bonds that will be possible to a single electronic chip, and the necessary on-chip electrical routing to the wirebond pads, will ultimately limit the electrical I/O to a VLSI circuit. But it is the precise performance tradeoffs between wire-bonding and flip-chip bonding of OE’s to VLSI that is the subject of this paper. There has been much previous work comparing optical interconnects, particularly in free-space optical configurations, with on-chip electrical interconnects. There has also been some work comparing optical interconnects to off-chip electrical interconnects at the chip-to-chip wafer, and MCM levels. Typically, these studies have assumed that the off-chip electrical interconnects can be treated either as purely capacitive lumped loads, or are limited by RC effects. These analyses are typically accurate for drivers with large source impedance and slow rise times so that all points on the line are at equipotential and line inductance can be ignored. In a somewhat more general case of perfectly matched long transmission lines, typical of MCM’s is also considered.

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T = T_{opt} + T_{conv}(P_{opt}) + T_{amp} + T_{elec} + T_{out}(P_{opt})
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Fig.1: Physical and functional schematic of a generic optoelectronic-VLSI Component.
Fig. 2. Photograph of the second CMOS/MQW-modulator foundry silicon wafer. The “6” wafer has multiple copies of a 17 mm x 17 mm 0.5x10^6 m CMOS.

However, as switching times reduce, RC line models are generally inadequate. Effects of wave propagation can commonly be seen on long lines. For short rise times, line inductance begins to cause ringing and overshoot even in short lines. Furthermore, the combination of large pad-capacitance and substantial wire-bond inductance that is characteristic of conventional wire-bonded chip-to-chip packaging has not specifically been treated. This configuration is one that is more consistent with low-cost packaging and signaling environments that are not impedance-controlled, and also with silicon VLSI technologies that may have driver-resistance that can vary considerably (tens of ohms to many kilo ohms) depending on the circuit design, and also to a lesser extent, from wafer to wafer for the same circuit. Here, the objective is to quantify the tradeoff between the speed and the power-dissipation of a wire-bonded OE transceiver versus a corresponding flip-chip bonded OE-VLSI transceiver [Fig. 2]. Assuming the line parameters and the load characteristics of the OE output device in each case are known, this question can be reformulated as a comparison between a wire-bonded electrical interconnect versus a flip chip bonded one for a given voltage swing required at the output, assumed here to be the full logic swing. This result can then be used to determine the power-speed tradeoffs of on chip versus off-chip optical transceivers and hence to quantify the benefits of intimate integration of optical transceivers onto.

5. CONCLUSION

This paper proposes a hierarchical method for VLSI circuit description and identifies a data construct which provides the necessary representation scheme to perform abstraction from low-level layouts to higher logical levels. The ANTISTROFEAS system is presented which is framework for VLSI reverse engineering based on visual. All-optical computing more than twenty years ago to the current research in optically interconnected electronics, the field of optical information processing has witnessed a shift of interest towards optoelectronic-VLSI systems.

Whereas optoelectronic devices have become reliable and show performance factors compatible with electronic processing, more work needs to be carried out on the integration aspects of this technology at the device, interfacing, system, assembly and testing levels.

Smart pixels, the integration of photo detector arrays and processing electronics on a single semiconductor chip, have been driven by its capability to perform parallel processing of large pixelated images and in real-time reduce a complex image into a manageable stream of signals that can be brought off-chip.

6. Future Direction

The major goals will be to achieve more compact packaging and to scale the SPAs to larger array dimensions. The former not only leads to smaller components, but shortens electrical connections within the SPA, thereby leading to higher potential speeds. It also supports the second goal since scaling can lead to excessively long electrical connections within the SPA for the current packaging methodology.

References

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